## ABSTRACT

The present invention discloses a non-volatile memory cell structure utilizing a charge trapping high-k dielectric in the place of the triple film stack (tunnel dielectric layer/charge trapping layer/blocking layer). The charge trapping characteristic of the high-k dielectric can be further improved by exposing the high-k dielectric layer to an treatment process such as a plasma exposure using excited state oxygen (e.g. oxygen plasma) ambient. By using a single layer as the charge trapping gate dielectric, the present invention presents a simple and inexpensive solution that permits device scaling to very small dimensions, together with the ease of device fabrication processes. The present invention also discloses the fabrication process for the charge trapping high-k gate dielectric non-volatile memory cell structure, applicable to bulk device, TFT device or SOI device.